REMARKS

Claims 1-18 are pending in the application. Claims 1, 4-7,10-13 and 16-18 have been amended. Applicants believe that this response addresses the Examiner's rejection and that any changes do not introduce new matter into the specification, limit the scope of the claims or result in any prosecution history estoppel.

Claim Discussion - 35 USC §112

The Examiner rejected claims 5, 6,11, 12, 17 and 18 under 35 USC §112, 2nd paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With respect to claim 5, "SMI-compatible task" has been replaced with "SMM-compatible task." Also, the proper antecedent basis has been provided for "SMI request."

With respect to claim 6, the proper antecedent basis has been provided for "SMI generation register." Also, "an SMM-compatible task" has been replaced with "the predefined SMM-compatible task."

The remaining claims have been amended accordingly.

Claim Discussion - 35 USC §101

The Examiner rejected claims 1-18 under 35 USC §101 on grounds that the claimed invention is directed to non-statutory subject matter. Applicants respectfully note that the claims have been amended to overcome this rejection. In particular, the claims have been amended to remove any references to executing a process.

Claim Discussion - 35 USC §102

The Examiner rejected claims 1 and 13 under 35 USC §102(b) as being anticipated by Hobson, US Patent No. 6,122,748. Applicants disagree with the Examiner's rejection. In particular, Hobson fails to generate a SMI request under ACPI control, change an operation mode of a processor to the SMM in response to the SMI request and execute a resume ACPI control process to return the processor to ACPI control after the predefined SMM-compatible task is complete as claimed or similarly claimed. As noted in the present application on page 6:

As shown in FIG. 2, when a complex task is encountered, the control method invokes a SMI from within ACPI code to handle operations in an optimal way (step 206). The chipset has a capability to generate an SMI based on accesses to predefined I/O address locations. The control method accesses the I/O address location that is programmed to trigger an SMI by using the chipset capability. An SMI is generated in the path of ASL code execution to enable usage of flexible native CPU instruction set within the SMI handler. A software SMI generation I/O register access is used to force an SMI occurrence within the ASL code execution path. In particular, an operation region is defined for the SMI I/O address that is being accessed. Once an operation region is defined for an I/O address, this newly defined entity can be accessed from within any of the control methods to generate an SMI.

Hobson fails to teach or suggest the claimed invention. In fact, Hobson teaches away since the BIOS is detecting whether a sleep enable bit is set. For example, Hobson, Column 5, lines 35-48 provides:

Next, the ACPI driver attempts to set the sleep enable field of the PM1b.sub.— CNT register which, for the reasons described above, writes the sleep enable bit pattern into the SMI command port (step 908). This time BIOS detects that the sleep enable bit is set (the 'yes' prong of step 904). BIOS then executes the necessary DEM routine to place the target device into the proper state for remote manageability (step 910), reconfigures the PM1a and PM1b registers for ACPI operation (step 912), and then enters the S3 sleep state (step 914). The program code executed to configure a device (step 912 of FIG. 9) for remote manageability will vary from device to device (e.g., a NIC versus a modem), and will typically be embodied in OEM supplied BIOS instructions.

Hobson, column 5, lines 54-62 provides:

Setting a WAK.sub.— STS flag triggers generation of a SCI which causes computer system 400 to wake-up in SMM (step 1000). Once PU 402 resumes execution, BIOS configures the target device for normal waking state operations (step 1002). Upon completing device configuration, the ACPI operating system is notified of the change in WAK.sub.— STS state via a SCI. Following SCI generation, control is returned to the ACPI driver which performs its normal wake-up sequence (step 1004).

Hobson, column 6, lines 60-64 provides:

entering a non-ACPI mode in response to the interrupt; configuring the device; and transitioning the computer system into a sleep state while in the non-ACPI mode.

As noted in page 4 of the present application:

Embodiments of the present invention provide for generation of SMI from ACPI ASL control method code to execute complex tasks including, but not limited to, transferring or searching through large amounts of data dynamically.

Instead of executing certain tasks using limited ASL functionality, a SMI is generated in an ASL code execution path to enable usage of a flexible native central processor unit (CPU) instruction set accessible to a system management mode (SMM) handler. In particular, an operation region is defined for a SMI generation VO register. The Pre-OS software configures the chipset to generate an SMI when an I/O access occurs to this particular address location defined through the ACPI Operation Region. An ACPI control method execution by any OS entity accesses the SMI generation I/O register to generate an SMI during ASL code execution when a predefined complex task is encountered, thus enabling the SMI handler code to advantageously execute the complex task. [Emphasis added]

In view of the above, Applicant respectfully notes that Hobson fails to teach or suggest the claimed invention. The claims should be allowed to issue.

Claim Discussion - 35 USC §103

The Examiner rejected claims 2, 3, 7-9, 14 and 15 under 35 USC §103(a) as being unpatentable over Hobsen in view of Intel [Intel's SL Enhanced Intel486 Microprocessor Family, June 1993]. Applicants respectfully disagree with the Examiner's rejection in view of the discussion above.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

If the Examiner has any questions, he is invited to contact the undersigned at (323) 654-8218. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

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Dated: September 6, 2006.

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I hereby certify that this paper is being transmitted online via EFS Web to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on September 6, 2006.

Margaux Rogriguez September 6, 2006